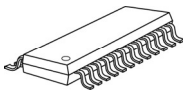
16 Channel Constant Current LED Driver with Current Gain and Ghosting Elimination

Features

- 16 constant-current output channels
- Constant output current invariant to load voltage change:
  Constant output current range:
  2-30mA@V_{DD}=5V;
  2-25mA@V_{DD}=3.3V
- Excellent output current accuracy:
  between channels: ±2.5% (max.)
  between ICs: ±3% (max.)
- Output current adjusted through an external resistor
- Fast response of output current, $\overline{OE}$ (min.): 50ns with good uniformity between output channels
- Integrating ghosting elimination
- 20MHz clock frequency
- Schmitt trigger input
- 4-bit current gain:25%~100%
- Double latch display function
- 3.3V/ 5V supply voltage
- “Pb-free & Green” Package

Shrink SOP



GP: SSOP24L-150-0.64

Quad Flat No-Lead

Product Description

With PrecisionDrive™ technology, MBI5125 is designed for LED displays which require to operate at low current and to match the luminous intensity of each channel. It provides supply voltage and accepts CMOS logic input at 3.3V and 5.0V to meet the trend of low power consumption. MBI5125 contains a serial buffer and data latches which convert serial input data into parallel output format. At MBI5125 output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks to drive LEDs within a large range of V_F variations. Moreover, MBI5125 integrates the pre-charge circuit which can relieve the LED ghosting effect.

MBI5125 provides users with great flexibility and device performance in their system design for LED display applications. The preset current of MBI5125 can be further programmed to 64 gain steps for LED global brightness adjustment, which gives users flexibility in controlling the light intensity of LEDs. MBI5125 guarantees to endure maximum 11V at the output port. The clock frequency of 20 MHz can also satisfy the system requirements of high volume data transmission.

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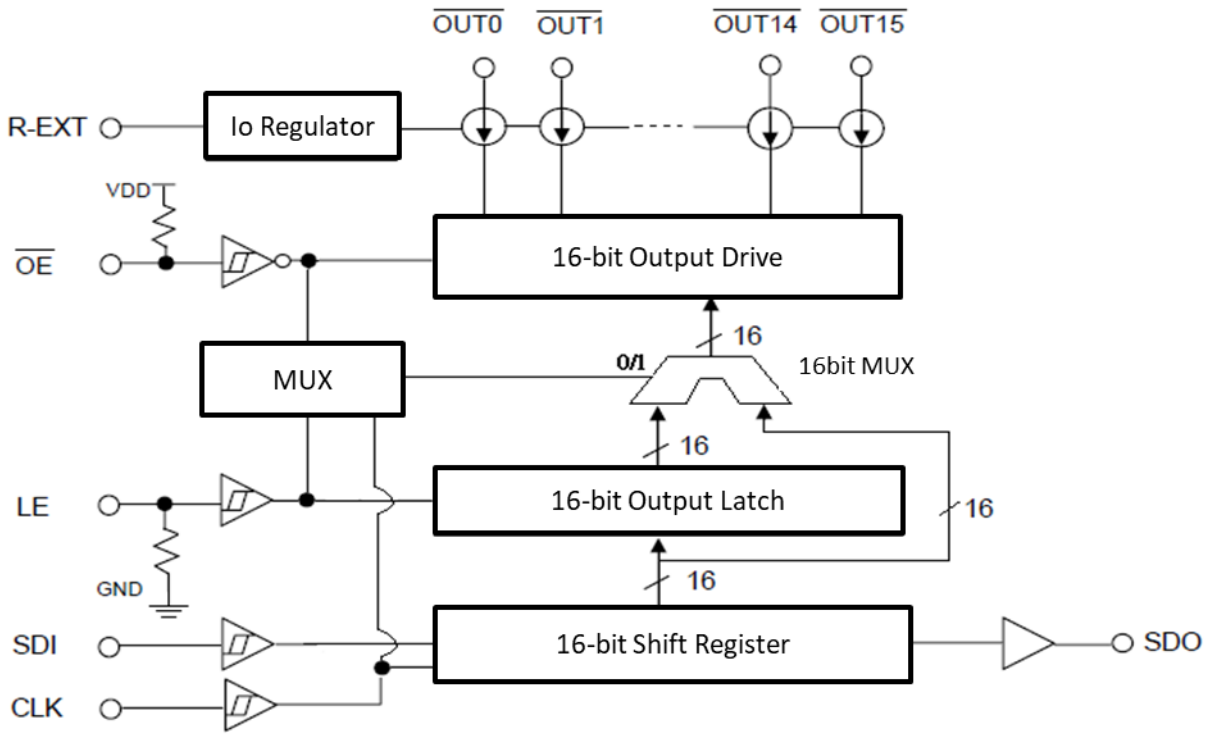
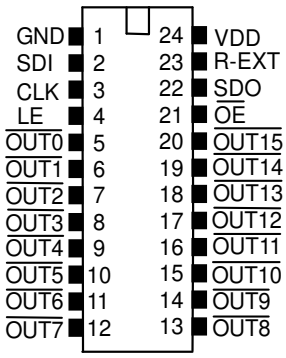
Block Diagram



Pin Configuration



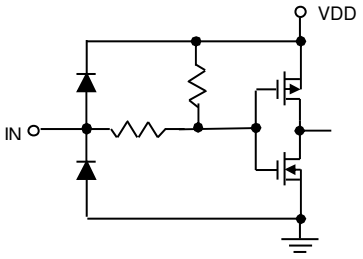
MBI5125GP

Terminal Description

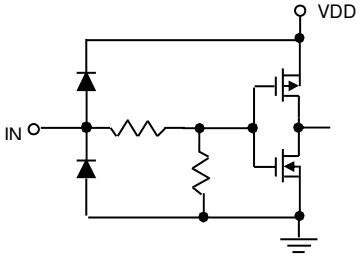
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
CLK	Clock input terminal for data shift on rising edge
LE	Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low.
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
$\overline{OE}$	Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
SDO	Serial-data output to the following SDI of next driver IC. SDO signal change on rising edge of CLK.
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

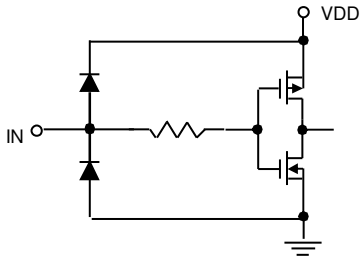
$\overline{OE}$ terminal



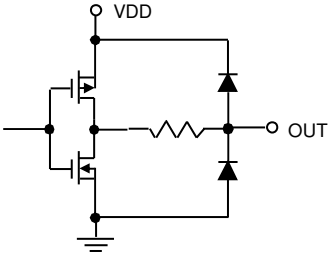
LE terminal



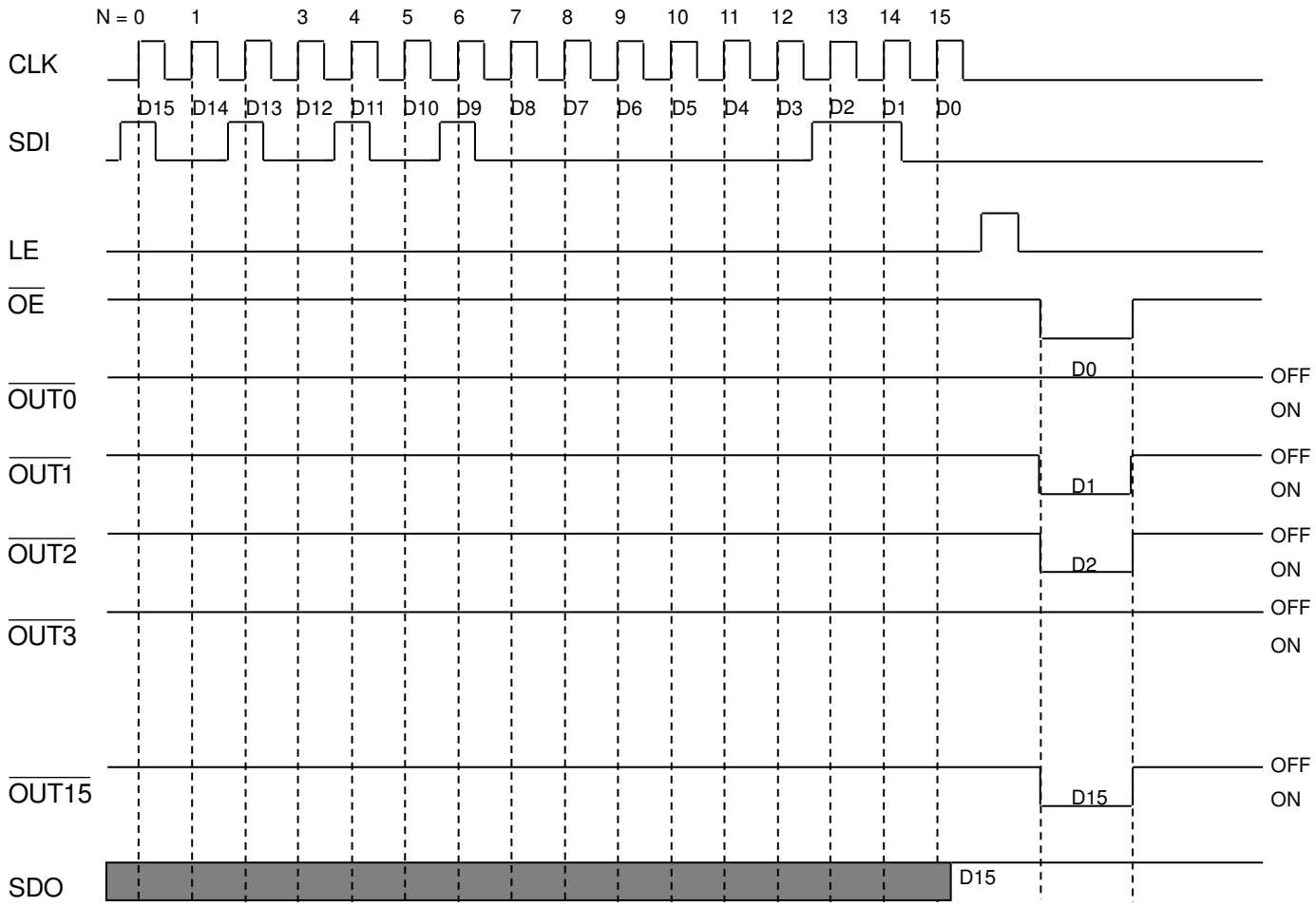
CLK, SDI terminal



SDO terminal



Timing Diagram



Truth Table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ ... $\overline{OUT7}$ ... $\overline{OUT15}$	SDO
↑	H	L	D_n	$\overline{D_n}$ ..... $\overline{D_{n-7}}$ .... $\overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ .... $\overline{D_{n-5}}$ .... $\overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ .... $\overline{D_{n-5}}$ .... $\overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+4}	Off	D_{n-13}

Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~5.5	V
Input Voltage(SDI, CLK, LE, GCLK)		V_{IN}	-0.4~V_{DD}+0.4	V
Output Current		I_{OUT}	+30	mA
Sustaining Voltage at OUT Port		V_{DS}	-0.5~+11	V
GND Terminal Current		I_{GND}	480	mA
Power Dissipation (On PCB, Ta=25°C)*	GP-type	P_D	1.76	W
Thermal Resistance (On PCB, Ta=25°C)*	GP-type	$R_{th(j-a)}$	70.90	°C/W
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	HBM(MIL-STD-883G Method 3015.7)	HBM	Class 3A (5000V)	
	MM(ANSI / ESD S5.2-2009)	MM	Class M4 (≧400V)	

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

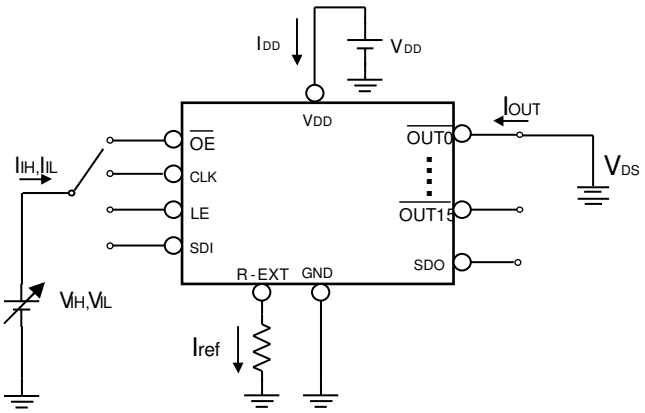
Electrical Characteristics (V_{DD}= 5.0V, Ta=25℃)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	5.5	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		2	-	30	mA
		I_{OH}	SDO , V_{OH}=4.6V		|-1.0|	-	-	mA
		I_{OL}	SDO, V_{OL} =0.4V		1.0	-	-	mA
Input Voltage	"H" level	V_{IH}	CLK , SDI , LE , /OE		0.75*V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	CLK , SDI , LE , /OE		GND	-	0.25*V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=5.5V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
Current Skew(Channel)		dI_{OUT1}	I_{OUT}=10mA V_{DS}=1.0V	R_{ext} =1845Ω	-	±1.5	±2.5	%
Current Skew(IC)		dI_{OUT2}	I_{OUT}=10mA V_{DS}=1.0V	R_{ext} =1845Ω	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation(one channel)		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.3	%/V
Output Current vs. Supply Voltage Regulation(one channel)		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±0.5	±1.0	%/V
PreCharge Voltage		Lvl-7	Bit[2:0]=111			3.82		V
		Lvl-6	Bit[2:0]=110			3.27		V
		Lvl-4	Bit[2:0]=100			3.03		V
		Lvl-0	Bit[2:0]=000			2.35		V
PreCharge Current		I_{preH}						mA
		IpreL						mA
AC Data dependent			Iout=10/3mA			3	5	%
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		74	113	167	KΩ
Pull-down Resistor		R_{IN}(down)	LE		74	113	167	KΩ

Electrical Characteristics (V_{DD}= 3.3V, Ta=25℃)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	5.5	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		2	-	25	mA
		I_{OH}	SDO , V_{OH}=2.9V		|-1.0|	-	-	mA
		I_{OL}	SDO, V_{OL} =0.4V		1.0	-	-	mA
Input Voltage	"H" level	V_{IH}	CLK , SDI , LE , /OE		0.75*V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	CLK , SDI , LE , /OE		GND	-	0.25*V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=5.5V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		2.9	-	-	V
Current Skew(Channel)		dI_{OUT1}	I_{OUT}=10mA V_{DS}=1.0V	R_{ext}=1845Ω	-	±1.5	±2.5	%
Current Skew(IC)		dI_{OUT2}	I_{OUT}=10mA V_{DS}=1.0V	R_{ext}=1845Ω	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation(one channel)		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.3	%/V
Output Current vs. Supply Voltage Regulation(one channel)		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	±0.5	±1.0	%/V
PreCharge Voltage		Lvl-7	Bit[2:0]=111			2.38		V
		Lvl-6	Bit[2:0]=110			1.9		V
		Lvl-4	Bit[2:0]=100			1.9		V
		Lvl-0	Bit[2:0]=000			1.57		V
PreCharge Current		I_{preH}						mA
		IpreL						mA
AC Data dependent								%
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		74	113	167	KΩ
Pull-down Resistor		R_{IN}(down)	LE		74	113	167	KΩ

Test Circuit for Electrical Characteristics



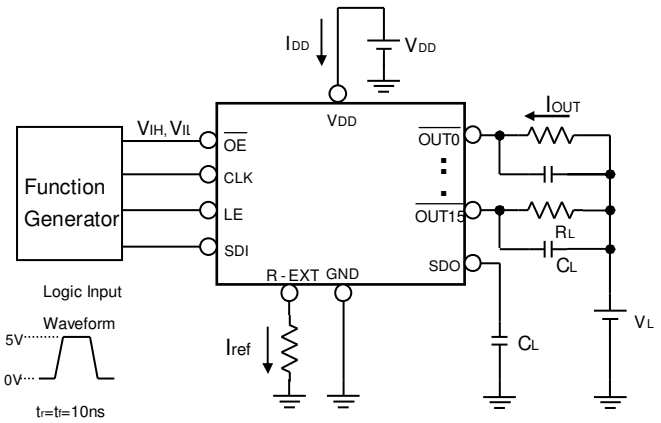
Switching Characteristics (V_{DD}= 5.0V , Ta=25 °C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	LE-$\overline{OUT0}$	t_{pLH2}	V_{DD}=5.0V V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1820Ω V_L=4.0V R_L=300Ω C_L=10pF	23	29	35	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}		19	24	29	ns
	CLK-SDO	t_{pLH}		23	29	35	ns
Propagation Delay Time ("H" to "L")	LE-$\overline{OUT0}$	t_{pHL2}		15	19	23	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pHL3}		19	25	31	ns
	CLK-SDO	t_{pHL}		22	28	34	ns
Staggered Delay of Output	$\overline{OUTn}$ - $\overline{OUTn+1}$	t_{stag}		-	2	-	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$ *	$t_{w(OE)}$		45	55	65	ns
Hold Time for LE		$t_{h(L)}$		5	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
SDO Rise Time		$t_{r,SDO}$		3	10	15	ns
SDO Fall Time		$t_{f,SDO}$		3	10	15	ns
Output Rise Time of Output Ports		t_{or}		25	30	39	ns
Output Fall Time of Output Ports		t_{of}		25	30	39	ns

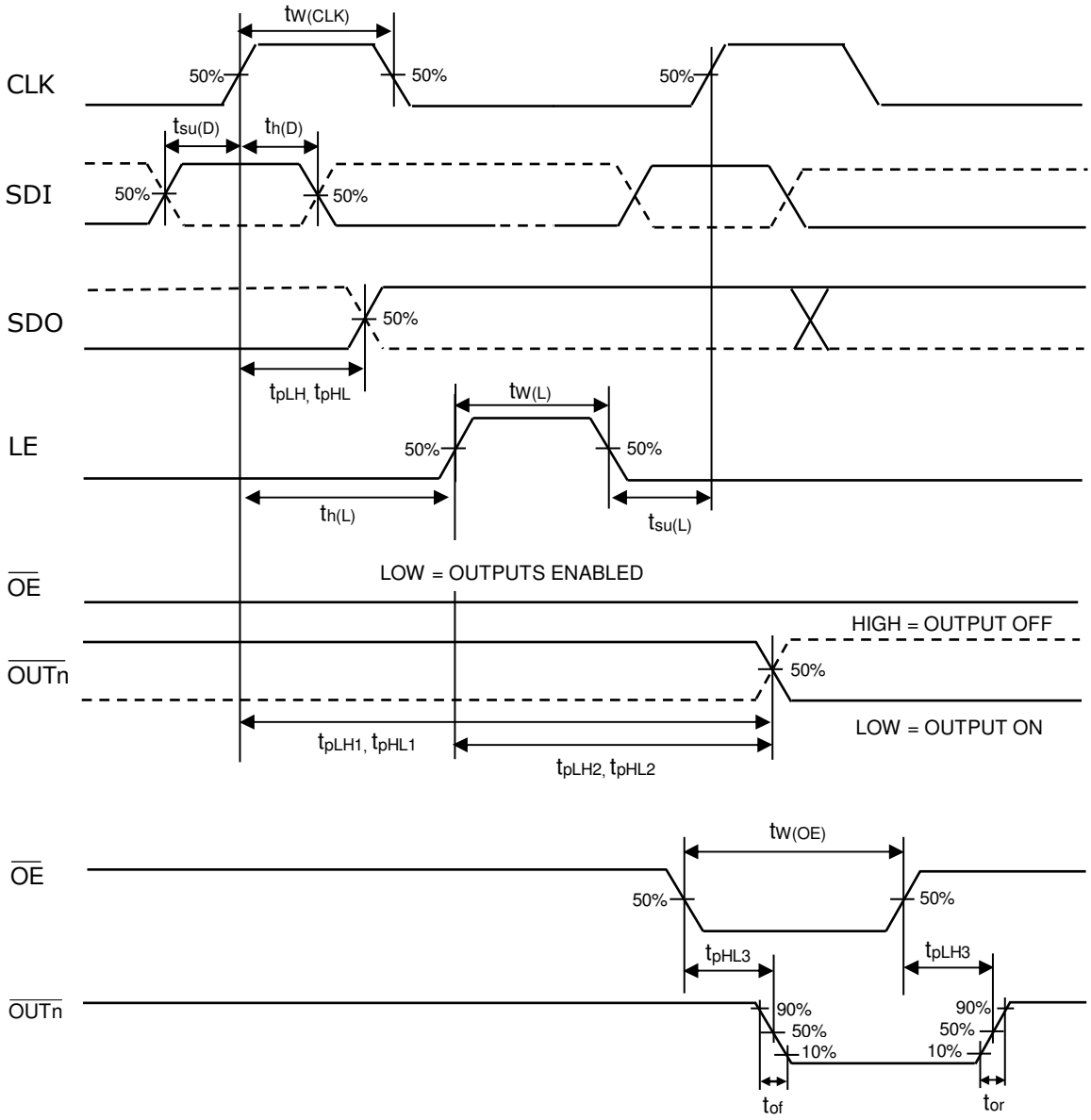
Switching Characteristics (V_{DD}= 3.3V , Ta=25 ºC)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	LE-$\overline{OUT0}$	t_{pLH2}	V_{DD}=3.3V V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1820Ω V_L=4.0V R_L=300Ω C_L=10pF	23	29	35	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}		29	37	45	ns
	CLK-SDO	t_{pLH}		34	42	50	ns
Propagation Delay Time ("H" to "L")	LE-$\overline{OUT0}$	t_{pHL2}		14	18	22	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pHL3}		22	28	34	ns
	CLK-SDO	t_{pHL}		32	40	48	ns
Staggered Delay of Output	$\overline{OUTn}$ - $\overline{OUTn+1}$	t_{stag}		-	2	-	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$ *	$t_{w(OE)}$		50	60	70	ns
Hold Time for LE		$t_{h(L)}$		5	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
SDO Rise Time		$t_{r,SDO}$		3	10	15	ns
SDO Fall Time		$t_{f,SDO}$		3	10	15	ns
Output Rise Time of Output Ports		t_{or}		25	30	40	ns
Output Fall Time of Output Ports		t_{of}		25	30	40	ns

Test Circuit for Switching Characteristics



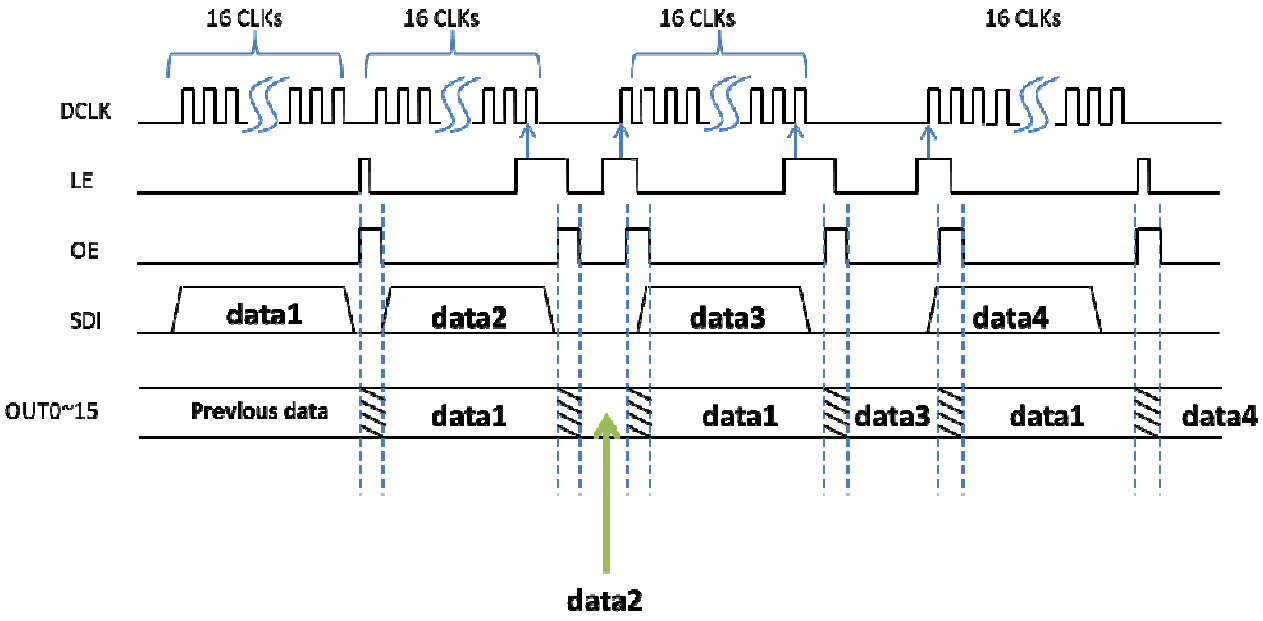
Timing Waveform



Control Command

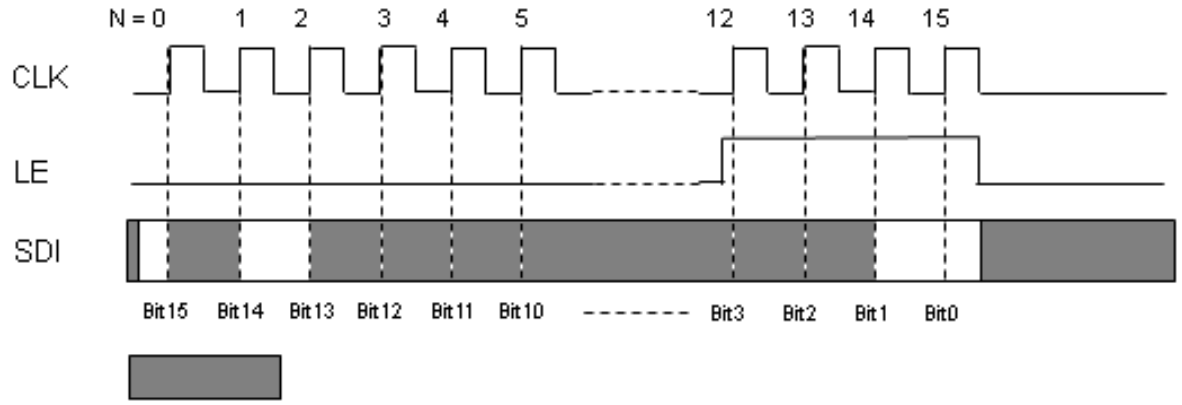
	Signals Combination	Description
Command Name	Number of CLK Rising Edge when LE is asserted	The action After a Falling Edge of LE
Latch data	0	Latch the serial data to the output latch. Latch the serial data to the driver's internal latch.
	1	Latch the serial data/Buffer data to the output latch.
Write configuration	4	Serial data are transferred to the "configuration register"
Read configuration	5	Serial data are transferred to the "configuration register"
No Action	2,3, >5	No action. Please do not use it.

Mux Mode



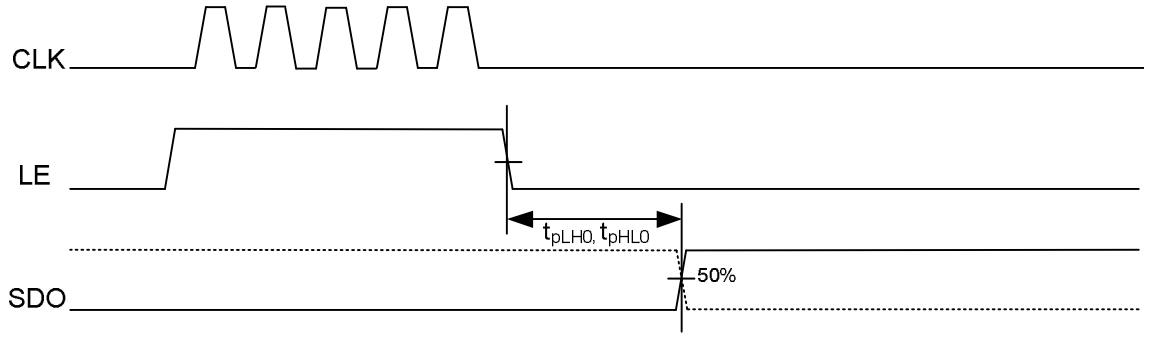
Waveform of Commands

Writing Configuration Register



After entering the writing configuration mode, the system controller sends a 16-bit configuration register setting to the 16-bit shift register through the SDI pin. Then the falling edge of LE will transfer the contents in the shift register to a 16-bit configuration register rather than the 16-bit output latch.

Read Configuration Register



Definition of Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Default

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1

Bit	Definition	Default Value	Function
F	Reserved	0	Reserved
E	Reserved	1	Reserved
D	Pre-charge Enable	1	0: Pre-Charge OFF, 1: Pre-Charge ON
C/B/A	Pre-charge voltage level selection	100	Values are simulated at VCC=5V 000: 2.35V 001: 2.45V 010: 2.64V 011: 2.84V 100: 3.03V (Default) 101: 3.21V 110: 3.28V 111: 3.83V
9	Reserved	0	Reserved
8	Reserved	0	Reserved
7	tr/tf selection	0	Values are simulated at VLED=4V, VCC=5V with 300ohm//10pF loading when iout=10mA and measured between 3.7V ~ 1.3V 0(high speed): tr/tf = 13.3ns / 24.8ns 1(low speed): tr/tf = 13.2ns / 38.3ns
6/5	Reserved	0	Reserved
4	Reserved	0	Reserved
3~0	Current gain	0000(Default)	cgadj = B[3]*16+B[2]*8+B[1]*4+B[0]*2 I(iout) = I(rext)*15*(10+cgadj/40) 0000~1111 = 25% ~ 100%

Default setting if configuration register is 16'h ED3F

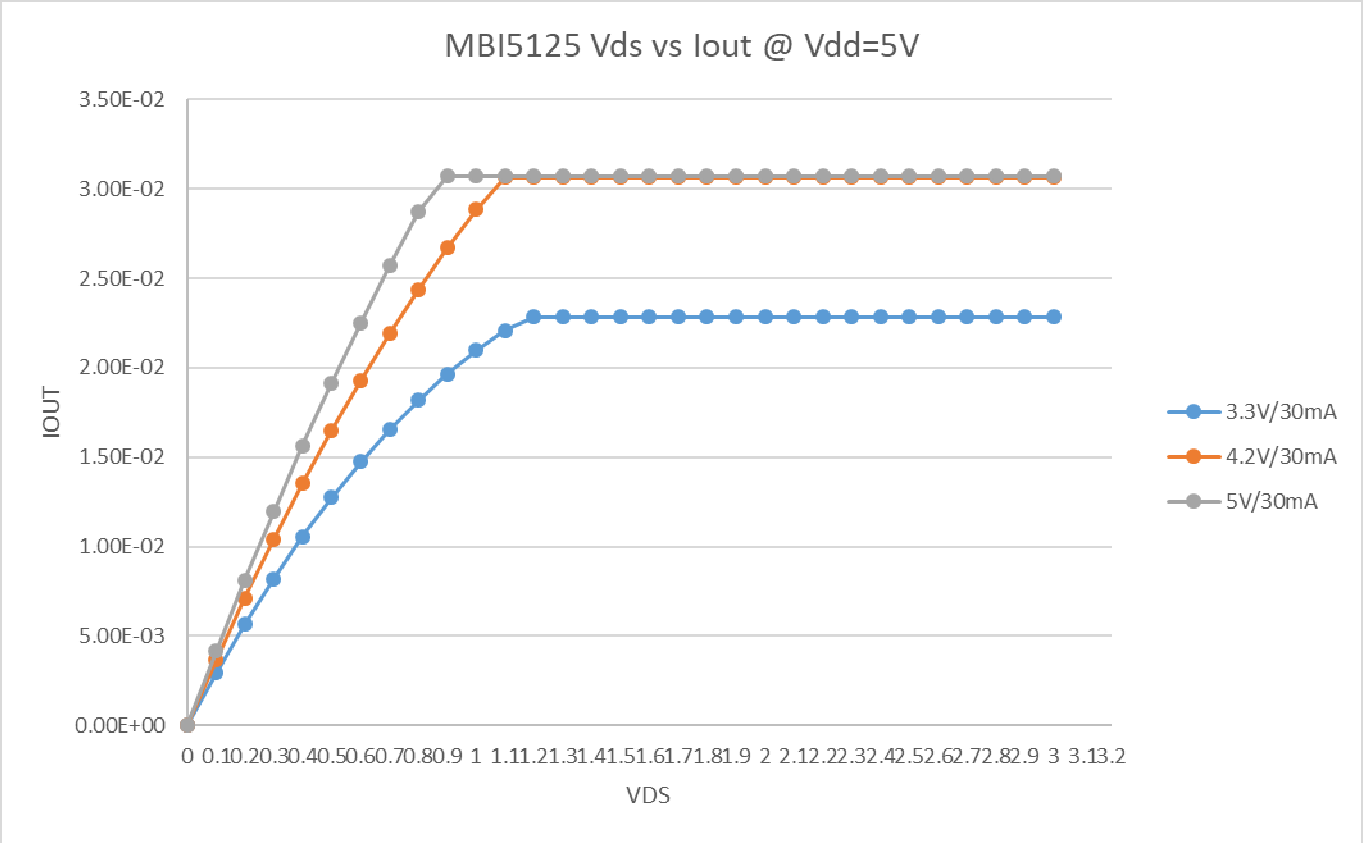
Application Information

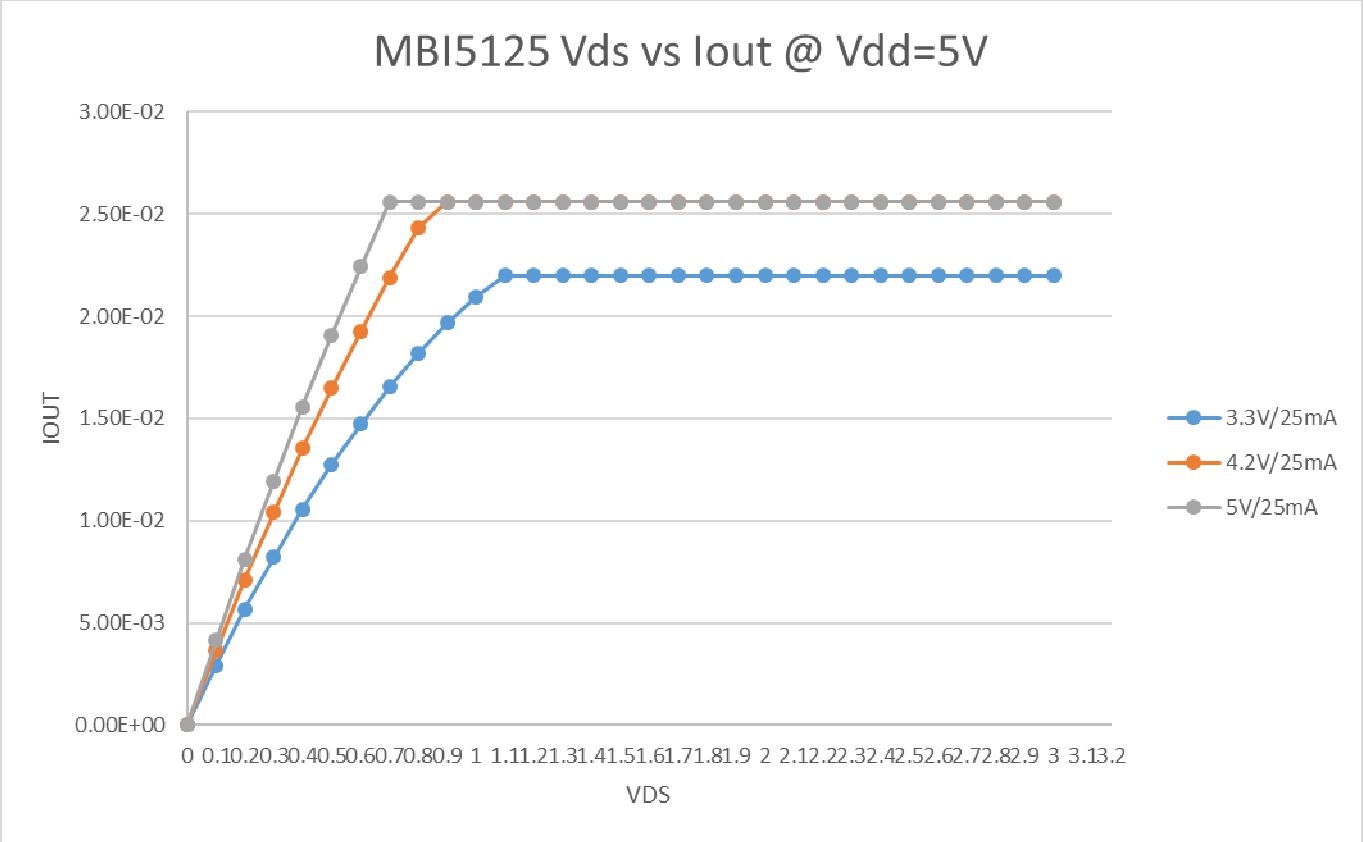
Constant Current

To design LED displays, MBI5125 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximum current variation between channels is less than ±2.5%, and that between ICs is less than ±3%.

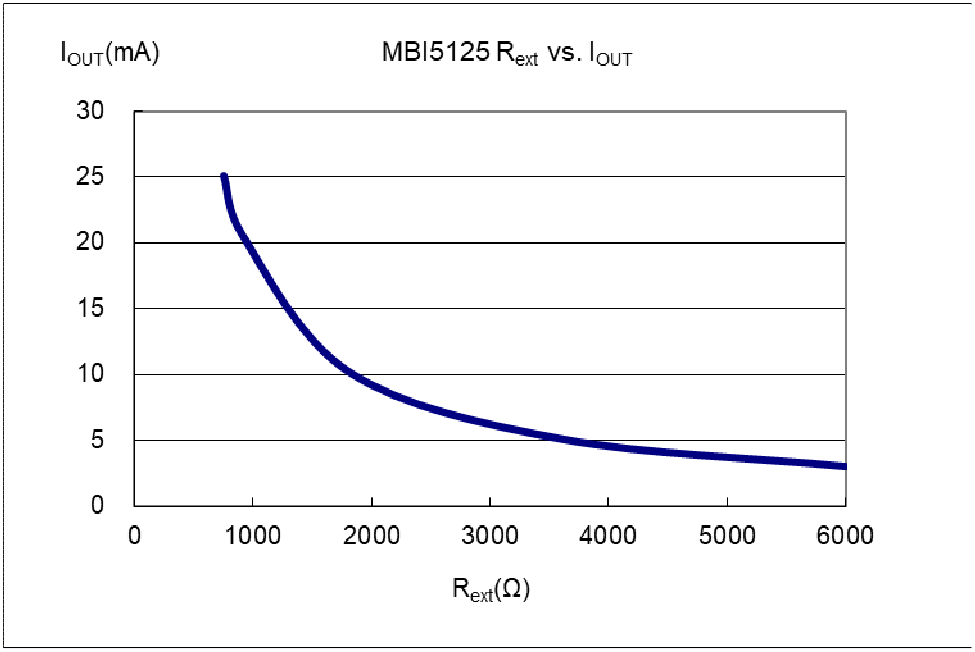
2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This performs as a perfection of load regulation.





Output current setting

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.



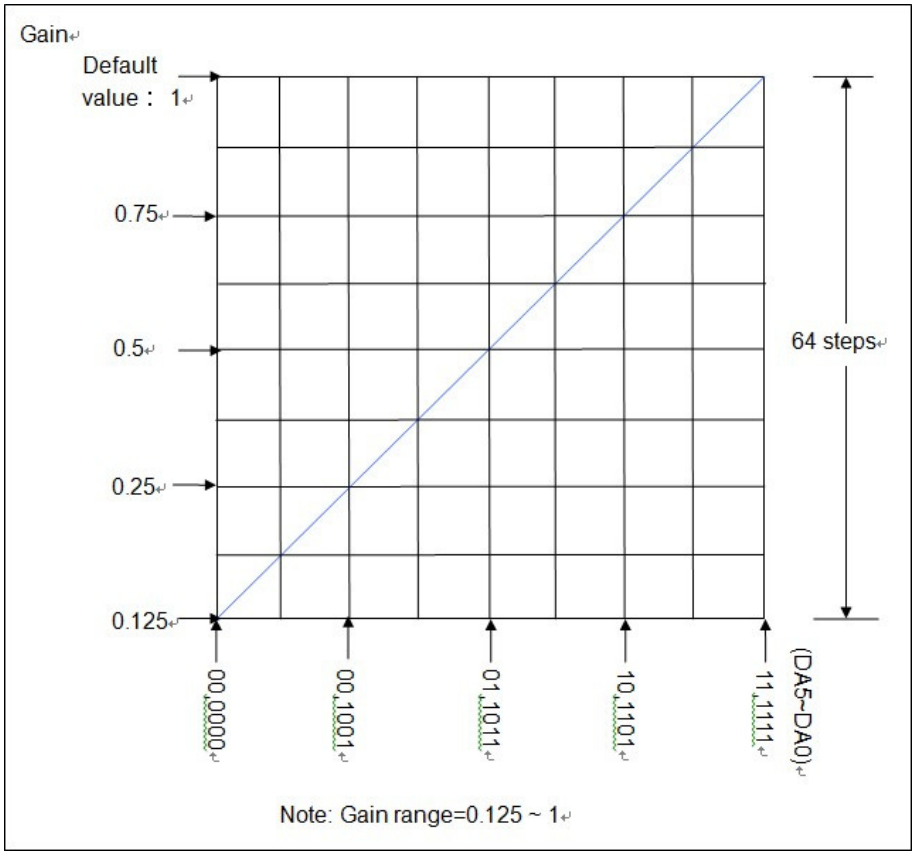
Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$ = 1.23Volt; I_{OUT} = ($V_{R\text{-}EXT}$ / R_{ext}) x 15 x G

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit 5 to bit 0 of the configuration register. The default value of G is 1. For your information, the output current is about 10mA when R_{ext}=1820Ω if G is set to default value 1.

The formula and the setting for G are described in the next section.

Current gain adjustment



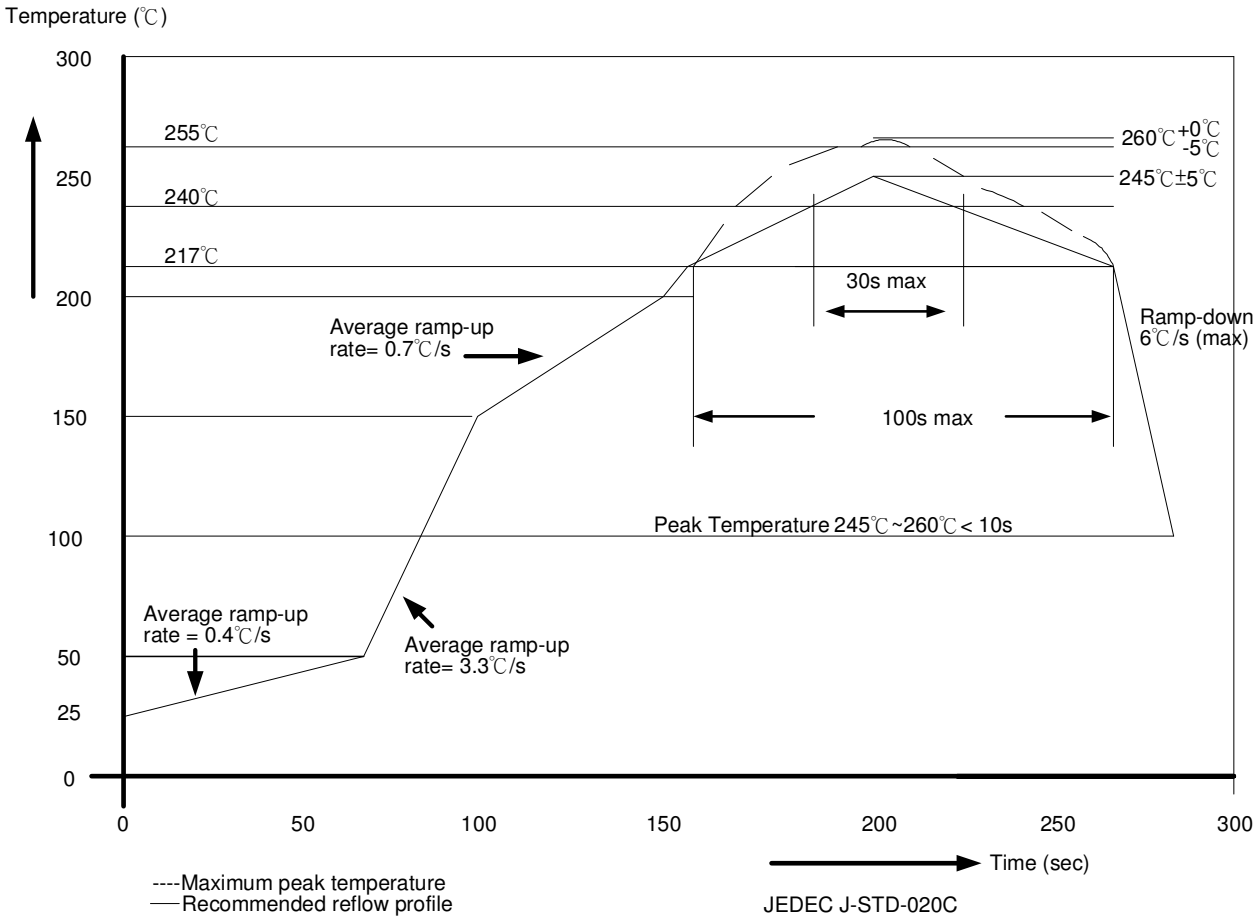
The 4 bits (bit 3~bit 0) of the configuration register set the gain of output current, i.e., G. As total 6-bit in number,
i.e., ranged from 6'b000000 to 6'b111111, these bits allow the user to set the output current gain up to 64 levels.
These bits can be further defined inside configuration register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	DA3	DA2	DA1	DA0

Bit 5 to bit 0 are DA5 ~ DA0.
The relationship between these bits and current gain G is:
G=0.125+(D/63)x0.875
and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:
$D= DA5x2^5+DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$
In other words, these bits can be looked as 6-bit mantissa DA5~DA0.
For example,
G=0.5, D=(0.5-0.125)/0.875x63=27
the D in binary form would be:
$D=27=0x2^5+1x2^4+1x2^3+0x2^2+1x2^1+1x2^0$
The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b011011.

Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with the higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.



Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

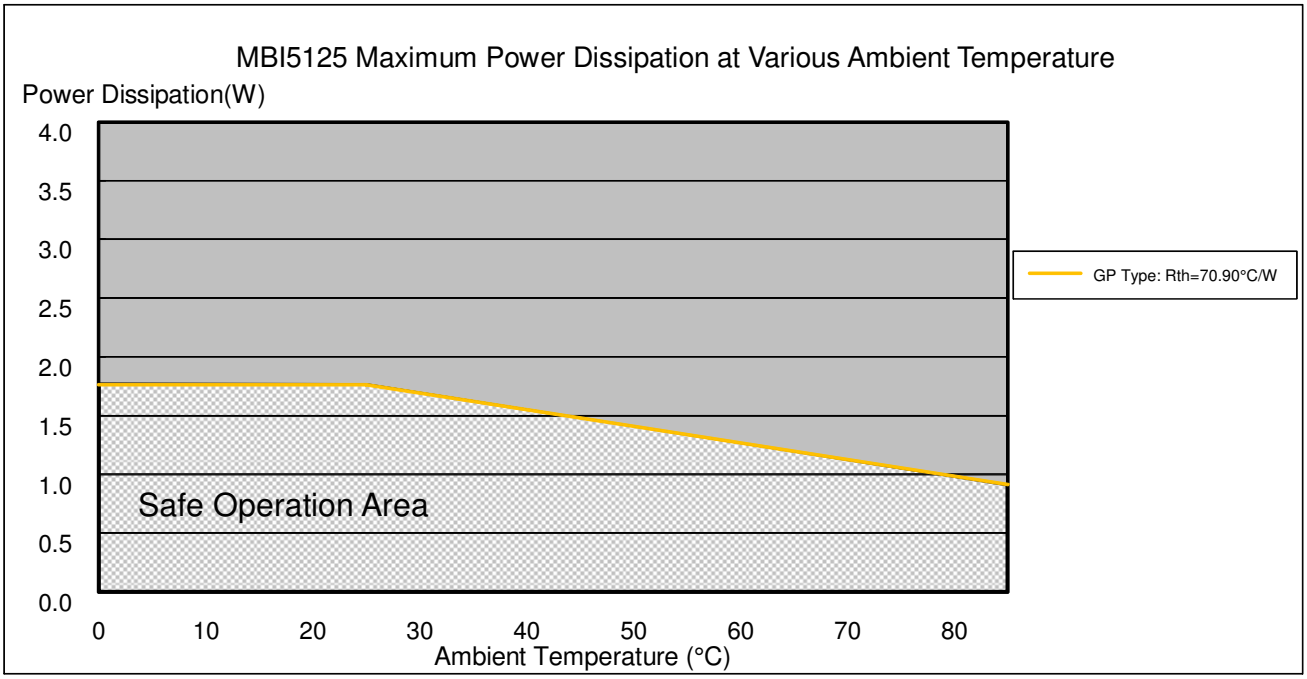
*For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Power Dissipation (P_D)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.

Package	$R_{th(j-a)}$ (°C/W)	P_D(W)
GP	70.90	1.76

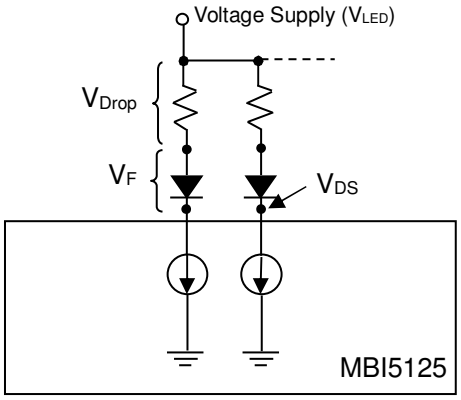


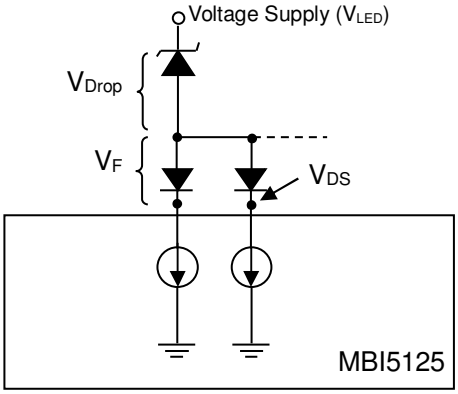
Load Supply Voltage (V_{LED})

MBI5125 are designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=2~30mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D(act)} > P_{D(max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

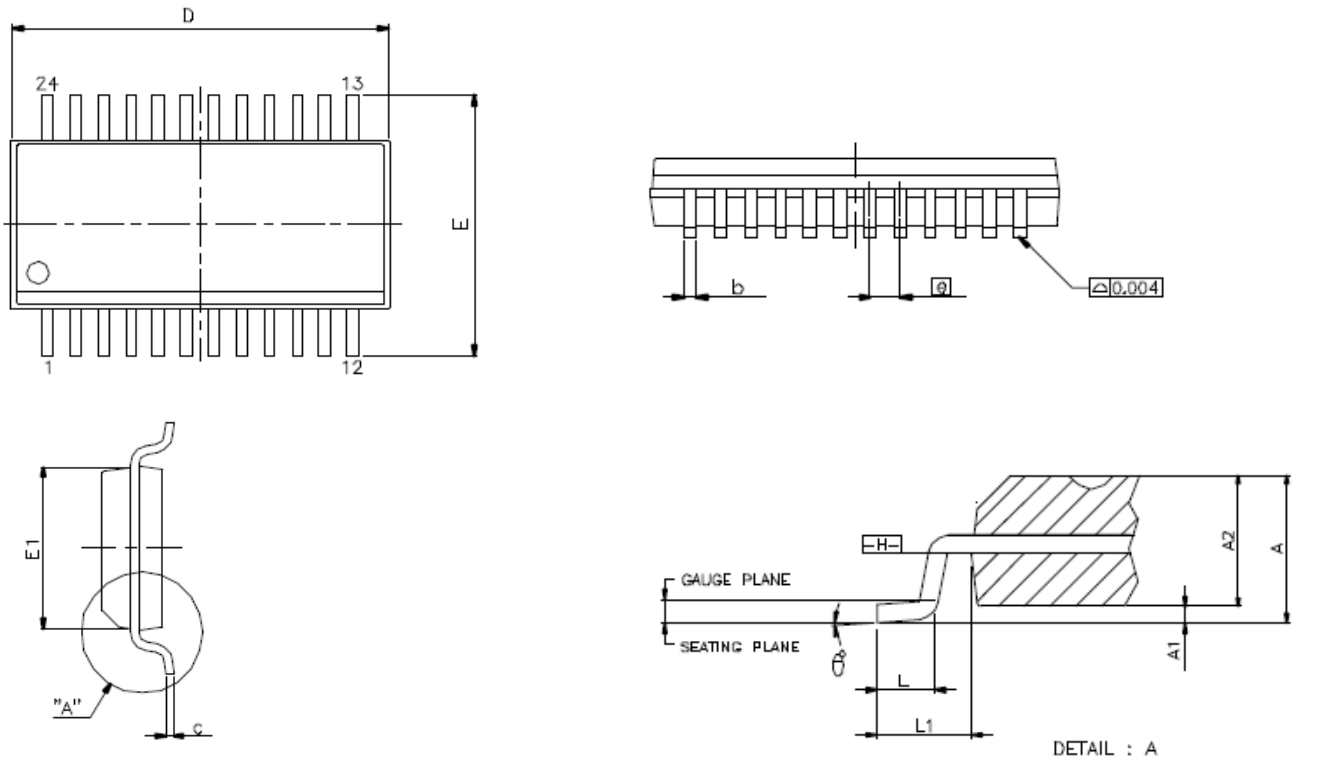
A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.





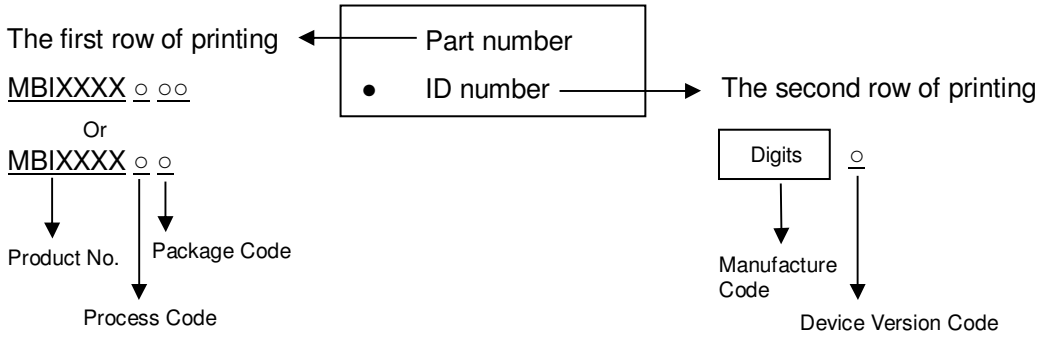
Package Outline



SYMBOLS	Dimensions shown in inches			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
θ °	0	—	8	0	—	8

MBI5125GP Outline Drawing

Product Top-mark Information



Product Revision History

Datasheet Version	Device Version Code
V0.01	T
V0.02	T
V0.03	T
V0.04	T

Product Ordering Information

Product Ordering Number*	RoHS Compliant Package Type	Weight (g)
MBI5125GP-T	SSOP24L-150-0.64	0.11

*Please place your order with the “product ordering number” information on your purchase order (PO).

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